

# TMC2011A/2111A

# Variable-Length Shift Register

### **Features**

- · Low power CMOS
- TMC2011A is a pin compatible replacement for the TDC1011 and TMC2011
- TMC2211A is a pin compatible replacement for the TMC2111
- · Inputs and outputs are TTL compatible
- DC-40MHz clock rate
- Selectable delay lengths (TMC2011A: 3 to 18 stages, TMC2111A: 1 to 16 stages)
- Special 4-bit wide mixed-delay mode (TMC2011A)
- Available in 24-pin CERDIP and plastic DIP and 28-lead Plastic Leadless Chip Carrier

## **Applications**

- Video filtering
- · High speed data registers
- Local storage registers
- · Digital delay lines
- · Television special effects
- · Pipeline register

## **Description**

The TMC2011A and TMC2111A are high-speed, byte-wide shift registers with programmable delay lengths.

The TMC2011A can be programmed to any length between 3 and 18 stages. It offers a special split-word mode which allows for mixed delay lengths. The TMC2011A, constructed in low-power CMOS, is pin and function compatible with the bipolar TDC1011.

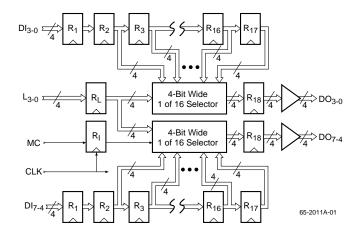
The TMC2111A is a byte-wide shift register that can be programmed to lengths of 1 to 16 stages.

The TMC2011A and TMC2111A are fully synchronous, with all operations controlled by a single master clock. Input and output registers are positive-edge triggered D-type flipflops. The length and mode controls are also registered. Both devices operate with a maximum clock rate of 40 MHz.

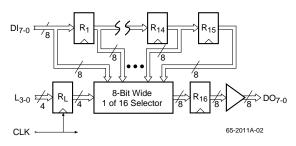
Fabricated in a submicron CMOS process, the TMC2011A and TMC2111A are TTL-compatible, and are available in 24-pin CERDIP and Plastic DIP packages as well as a 28-lead Plastic Leadless Chip Carrier.

## **Block Diagrams**

#### **TMC2011A**



### **TMC2111A**



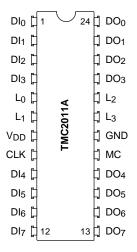
## **Functional Description**

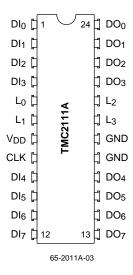
The TMC2011A consists of two 4-bit wide, programmable length shift registers. The TMC2111A consists of a single 8-bit wide, programmable length shift register. The internal

registers of each device share control signals and a common clock.

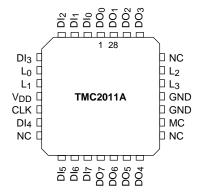
## **Pin Assignments**

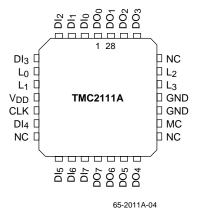
### 24 Lead DIP (B2, N2) Packages





### 28 Lead PLCC (R3) Package





# Pin Descriptions - TMC2011A

	Pin Number		
Pin Name	DIP	PLCC	Pin Function Description
Power		•	
V <sub>DD</sub>	7	8	<b>Supply Voltage.</b> The TMC2011A and operates from a single +5V supply. All power and ground lines must be connected.
GND	18	21,22	<b>Ground.</b> The TMC2011A operates from a single +5V supply. All power and ground lines must be connected.
Data Inputs	S	•	
DI <sub>7-0</sub>	12,11,10, 9,4,3,2,1	14,13,12, 10,5,4,3,2	<b>Data Input.</b> Eight inputs are provided for the data, which pass through the shift register unchanged. The eight inputs on the TMC2011A are divided into two groups of four bits to allow mixed delay operation. The lengths of these two groups are different when the Mode Control (MC) is HIGH (see Table 1). When MC is LOW both groups have equal delays.
Data Outpu	ıts	•	
DO7-0	13,14,15, 16,21,22, 23,24	15,16,17, 18,26,27, 28,1	<b>Data Output.</b> The outputs of the shift register are delayed relative to the input signals. The amount of the delay is programmable (see Table 1). The outputs remain valid for a minimum of tho nanoseconds after the leading edge of CLK. This allow the data to be latched into circuits with non-zero hold time requirements.
Controls		•	
CLK	8	9	<b>Master Clock.</b> All inputs and outputs are synchronous and operate from a single master clock. All operations occur on the rising edge of the master clock.
L <sub>3-0</sub>	19,20,6,5	23,24,7,6	<b>Length Select.</b> The length select input is used to determine the register delay of the TMC2011A. This input is registered and affects the output t <sub>DO</sub> after the clock edge after it is input to the device (see Timing Diagram). Delay lengths are specified in Table 1.
MC	17	20	<b>Mode Control.</b> The Mode Control is used to select the special 4-bit wide split mode. When HIGH, the delay on DO <sub>7-4</sub> is fixed at 18 stages, while DO <sub>3-0</sub> have the delay specified by the length select. When MC is LOW, all eight bits have equal delays as specified by the length select.

# Pin Descriptions - TMC2111A

	Pin Number n Name DIP PLCC		
Pin Name			Pin Function Description
Power			
VDD	7	8	<b>Supply Voltage.</b> The TMC2111A operates from a single +5V supply. All power and ground lines must be connected.
GND	17,18	20,21,22	<b>Ground.</b> The TMC2111A operates from a single +5V supply. All power and ground lines must be connected.
Data Inputs	<b>,</b>		
DI <sub>7-0</sub>	12,11,10, 9,4,3,2,1	14,13,12, 10,5,4,3,2	<b>Data Input.</b> Eight inputs are provided for the data, which pass through the shift register unchanged. The TMC2111A consists of a single group of eight bits with all data bits having equal delays.
Data Outpu	its		
DO <sub>7-0</sub>	13,14,15, 16,21,22, 23,24	15,16,17, 18,26,27, 28,1	<b>Data Output.</b> The outputs of the shift register are delayed relative to the input signals. The amount of the delay is programmable (see Table 1). The outputs remain valid for a minimum of tho nanoseconds after the leading edge of CLK. This allow the data to be latched into circuits with non-zero hold time requirements.
Controls	•		
CLK	8	9	<b>Master Clock.</b> All inputs and outputs are synchronous and operate from a single master clock. All operations occur on the rising edge of the master clock.
L3-0	19,20,6,5	23,24,7,6	<b>Length Select.</b> The length select input is used to determine the register delay of the TMC2111A. This input is registered and affects the output tDO after the clock edge after it is input to the device (see Timing Diagram). Delay lengths are specified in Table 1.

**Table 1. Programming Length Controls** 

	TMC2011A								
	Input	Code		Mode (	Mode (MC) =0 Mode (MC) =1		Mode (MC) =0 Mode (MC) =1 Th		TMC2111A
L <sub>3</sub>	L <sub>2</sub>	L <sub>1</sub>	L <sub>0</sub>	DO <sub>3-0</sub> Length	DO <sub>7-4</sub> Length	DO <sub>3-0</sub> Length	DO <sub>7-4</sub> Length	DO <sub>7-0</sub> Length	
0	0	0	0	3	3	3	18	1	
0	0	0	1	4	4	4	18	2	
0	0	1	0	5	5	5	18	3	
0	0	1	1	6	6	6	18	4	
0	1	0	0	7	7	7	18	5	
0	1	0	1	8	8	8	18	6	
0	1	1	0	9	9	9	18	7	
0	1	1	1	10	10	10	18	8	
1	0	0	0	11	11	11	18	9	
1	0	0	1	12	12	12	18	10	
1	0	1	0	13	13	13	18	11	
1	0	1	1	14	14	14	18	12	
1	1	0	0	15	15	15	18	13	
1	1	0	1	16	16	16	18	14	
1	1	1	0	17	17	17	18	15	
1	1	1	1	18	18	18	18	16	

## **Absolute Maximum Ratings**

(beyond which the device may be damaged)<sup>1</sup>

Parameter	Min	Тур	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V <sub>DD</sub> + 0.5	V
Output, Applied Voltage <sup>2</sup>	-0.5		V <sub>DD</sub> + 0.5	V
Output, Externally Forced Current <sup>3,4</sup>	-3.0		6.0	mA
Output, Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating, Ambient Temperature	-20		110	°C
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering (10 seconds)			300	°C

#### Notes:

- 1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
- 2. Applied voltage must be current limited to specified range.
- 3. Forcing voltage must be limited to specified range.
- 4. Current is specified as conventional current flowing into the device.

# **Operating Conditions**

Param	Parameter			Nom	Max	Units
V <sub>DD</sub>	Power Supply Voltage		4.75	5.0	5.25	V
fCLK	Clock frequency	TMC2011A, 2111A			30	MHz
		TMC2011A-1, 2111A-1			40	
tPWH	CLK pulse width, HIGH		12			ns
tpwL	CLK pulse width, LOW		12			ns
ts	Input Data Set-up Time		6			ns
tH	Input Data Hold Time		1			ns
VIH	Input Voltage, Logic HIGH	DI7-0, L3-0, MC	2.0			V
		CLK	2.6			
VIL	Input Voltage, Logic LOW				0.8	V
Іон	Output Current, Logic HIGH				-2.0	mA
loL	Output Current, Logic LOW				4.0	mA
TA	Ambient Temperature, Still Air		0		70	°C

## **Electrical Characteristics**

Param	eter	Conditions	Min	Тур	Max	Units
IDDU	Power Supply Current, Unloaded	V <sub>DD</sub> = Max, f <sub>CLK</sub> =30 MHz V <sub>DD</sub> = Max, f <sub>CLK</sub> =40 MHz			30 40	mA mA
IDDQ	Power Supply Current, Quiescent	VDD = Max, CLK = LOW			0.5	mA
CPIN	I/O Pin Capacitance			5		pF
ΙΗ	Input Current, HIGH	VDD = Max, VIN = VDD			±10	μΑ
Iμ	Input Current, LOW	V <sub>DD</sub> = Max, V <sub>IN</sub> = 0 V			±10	μΑ
los	Short-Circuit Current				-100	mA
Voн	Output Voltage, HIGH	DO <sub>7-0</sub> , I <sub>OH</sub> = Max	2.4			V
VoL	Output Voltage, LOW	DO <sub>7-0</sub> , I <sub>OL</sub> = Max			0.4	V

# **Switching Characteristics**

Parameter		Conditions	Min	Тур	Max	Units
tDO	Output Delay Time	CLOAD = 25 pF			15	ns
tHO	Output Hold Time	CLOAD = 25 pF	3			ns

## **Timing Diagrams**

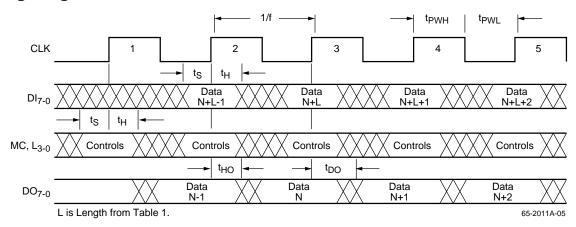


Figure 1. Preset Length Controls

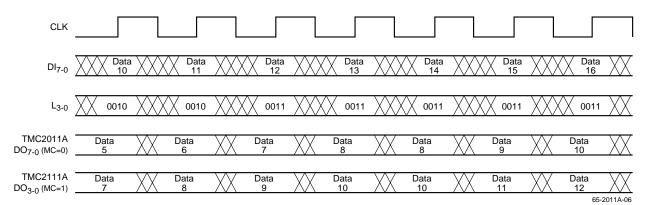


Figure 2. Length Control Operation

## **Equivalent Circuits**

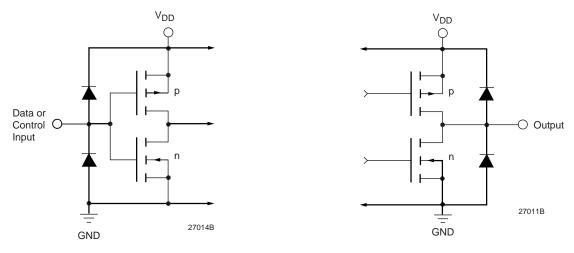


Figure 3. Equivalent Digital Input Circuit

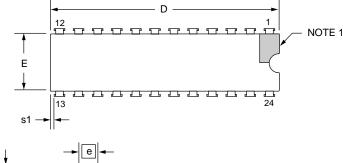
Figure 4. Equivalent Digital Output Circuit

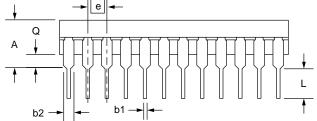
### **Mechanical Dimensions**

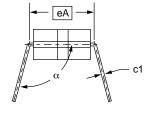
### 24-Lead Ceramic DIP Package

Cumbal	Inches		Millim	Notes	
Symbol	Min.	Max.	Min.	Max.	Notes
Α	_	.200	_	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D		1.280	_	32.51	4
Е	.220	.310	5.59	7.87	4
е	.100	.100 BSC		BSC	5
eA	.300	BSC	7.62	BSC	7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	_	.13	_	6
α	90°	105°	90°	105°	

- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13 and 24 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
- 6. Applies to all four corners (leads number 1, 12, 13, and 24).
- "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "a" is 90°.
- 8. All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Twenty-two spaces.





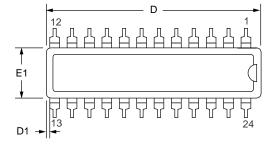


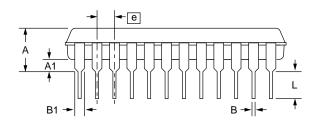
## **Mechanical Dimensions** (continued)

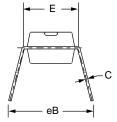
## 24-Lead Plastic DIP Package

Symbol	Inc	hes	Millin	Notes	
	Min.	Max.	Min.	Max.	Notes
Α	_	.210	_	5.33	
A1	.015		.38	_	
A2	.115	.195	2.53	4.95	
В	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
С	.008	.015	.20	.38	4
D	1.125	1.275	28.58	32.39	2
D1	.005		.13	_	
Е	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
е	.100	BSC	2.54 BSC		
eB	_	.430	_	10.92	
_L	.115	.160	2.92	4.06	
N	24		2	5	

- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- 3. Terminal numbers are shown for reference only.
- 4. "C" dimension does not include solder finish thickness.
- 5. Symbol "N" is the maximum number of terminals.





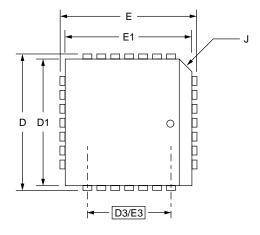


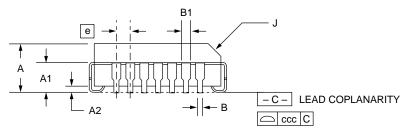
## **Mechanical Dimensions** (continued)

## 28-Lead PLCC Package

Cumbal	Inc	hes	Millin	Notes	
Symbol	Min.	Max.	Min.	Max.	Notes
Α	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	_	.51	_	
В	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300	BSC	7.62	BSC	
е	.050	BSC	1.27	BSC	
J	.042	.048	1.07	1.22	2
ND/NE	-	7	7		
N	2	8	28		
ccc	_	.004	_	0.10	

- 1. All dimensions and tolerances conform to ANSI Y14.5M-1982
- 2. Corner and edge chamfer (J) =  $45^{\circ}$
- 3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)





## **Ordering Information**

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2011AB2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" CerDIP	2011AB2C
TMC2011AB2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" CerDIP	2011AB2C1
TMC2011AN2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" Plastic DIP	2011AN2C
TMC2011AN2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" Plastic DIP	2011AN2C1
TMC2011AR3C	0°C to 70°C	30 MHz	Commercial	28 Lead PLCC	2011AR3C
TMC2011AR3C1	0°C to 70°C	40 MHz	Commercial	28 Lead PLCC	2011AR3C1
TMC2111AB2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" CerDIP	2111AB2C
TMC2111AB2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" CerDIP	2111AB2C1
TMC2111AN2C	0°C to 70°C	30 MHz	Commercial	24 Pin 0.3" Plastic DIP	2111AN2C
TMC2111AN2C1	0°C to 70°C	40 MHz	Commercial	24 Pin 0.3" Plastic DIP	2111AN2C1
TMC2111AR3C	0°C to 70°C	30 MHz	Commercial	28 Lead PLCC	2111AR3C
TMC2111AR3C1	0°C to 70°C	40 MHz	Commercial	28 Lead PLCC	2111AR3C1

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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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